## AMENDMENTS TO THE CLAIMS

1. (Original) A process of fabricating a flash memory cell array, comprising the steps of: forming a source diffusion between two bit line diffusions in a substrate, forming stacked pairs of control gates and floating gates on the substrate on opposite sides of the source diffusion, with each stacked pair having a control gate positioned above a floating gate, forming an erase gate on the substrate between the stacked pairs, and forming select gates on the substrate between the stacked pairs and the bit line diffusions.

2. (Original) The process of Claim 1 wherein the source diffusion is formed after the stacked pairs of control gates and floating gates are formed.

3. (Original) The process of Claim 1 wherein the source diffusion is formed by ion implantation.

4. (Original) The process of Claim 3 wherein the ion implantation is done with dopants selected from the group consisting of $P^{31}$ and $As^{75}$.

5. (Original) The process of Claim 1 wherein the bit line diffusions are formed after the select gates are formed.

6. (Original) The process of Claim 1 wherein the bit line diffusions are formed by ion implantation.

7. (Original) The process of Claim 6 wherein the ion implantation is done with dopants selected from the group consisting of $P^{31}$ and $As^{75}$.

8. (Original) The process of Claim 1 wherein the floating gates and the control gates are formed by depositing a first layer of silicon on the substrate, forming a second layer of silicon above the first layer, removing portions of the second layer to form the control gates, and removing portions of the first layer to form the floating gates.

9. (Original) The process of Claim 8 wherein the portions of the first and second layers of silicon are removed by etching.

10. (Original) The process of Claim 1 wherein the erase gate and the select gates are formed by depositing a layer of silicon over, between and beside the stacked gates, and removing the portions of the silicon above the stacked gates and above the bit line diffusions.

11. (Original) The process of Claim 10 wherein the bit line diffusions are formed after the select gates are formed.

12. (Original) The process of Claim 1 including the steps of forming a relatively thin tunnel oxide between the floating gates and the substrate, a first relatively thick dielectric between the floating gates and the select and erase gates, and a second relatively thick dielectric between floating gates and control gates.

13. (Original) The process of Claim 1 including the steps of forming relatively thin tunnel oxides between the each of the floating gates and the substrate, forming a first relatively thick dielectric between the floating gates and the select and erase gates, and forming a second relatively thick dielectric between the floating gate and the control gate in each pair of stacked gates.

14. (Original) The process of Claim 1 including the steps of forming bit line lines which cross over the stacked gates, the select gates, and the erase gate, and forming bit line contacts which interconnect the bit line diffusions and the bit lines.

15. (Original) The process of Claim 1 wherein the stacked gates and the source diffusion are formed in such manner that the floating gates partly overlie the source diffusion.

16. (Original) The process of Claim 1 wherein the select gates and the bit line diffusions are formed in such manner that the select gates partly overlie the bit line diffusions.

17. (Currently Amended) A process of fabricating a flash memory cell, comprising the steps of:

forming a vertically stacked pair of floating and control gates on a substrate, with the control gate being positioned above and aligned with the floating gate,

forming a source diffusion in the substrate on one side of the stacked pair,

forming an erase gate above the source diffusion on the one side of the stacked pair,

forming a select gate on a second side of the stacked pair, and

forming a bit line diffusion in the substrate near the select gate.

18. (Currently Amended) The process of Claim 17 including the steps of

forming a bit line which crosses above the vertically stacked pair, the erase gate and the select gate, and

forming a bit line contact which interconnects the bit line diffusion and the bit line.

19. (Original) The process of Claim 17 including the steps of forming a relatively thin tunnel oxide between the floating gate and the substrate, a first relatively thick dielectric between the floating gate and the select and erase gates, and a second relatively thick dielectric between the floating gate and the control gate.

20. (Original) A process of fabricating a flash memory cell array, comprising the steps of: forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, forming a first dielectric film over the first silicon layer, forming a second silicon layer on the first dielectric film, forming a second dielectric film on the second silicon layer, etching away portions of the second silicon layer and the second dielectric film to form control gates, etching away portions of the first layer of silicon and the first dielectric film to form floating gates which are stacked beneath and self-aligned with control gates, forming source regions in the active area between the stacked gates, forming a third dielectric film on the side walls of the control and floating gates and on the active area of the silicon substrate, depositing a third silicon layer over the third dielectric film, removing portions of the third silicon layer to form select and erase gates on opposite sides of the stacked gates, with the erase gates being positioned directly above the source regions, forming bit line diffusions in the active area of the substrate which are partially overlapped by the select gates, and forming bit line lines

which extend above the gates and bit line contacts which interconnect the bit lines and the bit line diffusions.

21. (Original) A process of fabricating a flash memory cell array, comprising the steps of: forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, etching away portions of the first silicon layer to form spaced apart rows of silicon which extend in a first direction on the substrate, forming a first dielectric film over the rows of silicon, forming a second silicon layer on the first dielectric film, forming a second dielectric film on the second silicon layer, etching away portions of the second silicon layer and the second dielectric film to form control gates with exposed side walls which extend in a direction perpendicular to the rows of silicon, etching away portions of the rows of silicon and the first dielectric film to form floating gates which are stacked beneath and self-aligned with control gates, forming source regions in the active area of the substrate between the stacked gates, forming a third dielectric film on the side walls of the control and floating gates and on the active area of the silicon substrate, depositing a third silicon layer over the third dielectric film, removing portions of the third silicon layer to form select and erase gates on opposite sides of the stacked gates, with the erase gates being positioned directly above the source regions, forming bit line diffusions in the active area of the substrate which are partially overlapped by the select gates, and forming bit line lines which extend in the first direction above the gates and bit line contacts which interconnect the bit lines and the bit line diffusions.

22. (Previously Added) The process of Claim 17 wherein a second bit line diffusion is formed in the substrate, the source diffusion is formed between the two bit line diffusions, stacked pairs of control gates and floating gates are formed on the substrate on opposite sides of the source diffusion, with each stacked pair having a control gate positioned above a floating gate, the erase gate is formed between the stacked pairs, and select gates are formed between the stacked pairs and the bit line diffusions.

23. (Previously Added) The process of Claim 17 wherein the substrate is a silicon substrate;

the stacked pair of floating and control gates is formed by forming an oxide layer on an active area in the substrate, forming a first silicon layer on the oxide layer, forming a first dielectric film over the first silicon layer, forming a second silicon layer on the first dielectric film, forming a second dielectric film on the second silicon layer, etching away portions of the second dielectric film and the second silicon layer to form the control gate, and etching away portions of the first layer of silicon and the first dielectric film to form the floating gate which is thereby self-aligned with the control gate;

the source diffusion is formed in the active area of the substrate;

the select and erase gates are formed by forming a third dielectric film on the side walls of the control and floating gates and on the active area of the substrate, depositing a third silicon layer over the third dielectric film, and removing portions of the third silicon layer to form the select gate and the erase gates, with the erase gate being positioned directly above the source diffusion;

the bit line diffusion is formed in the active area of the substrate and is partially overlapped by the select gate;

a bit line is formed above the gates; and

a bit line contact is formed to interconnect the bit line and the bit line diffusion.

24. (Previously Added) The process of Claim 17 wherein

the substrate is a silicon substrate;

the stacked pair of floating and control gates is formed by forming an oxide layer on an active area in a silicon substrate, forming a first silicon layer on the oxide layer, etching away portions of the first silicon layer to form spaced apart rows of silicon which extend in a first direction on the substrate, forming a first dielectric film over the rows of silicon, forming a second silicon layer on the first dielectric film, forming a second dielectric film on the second silicon layer, etching away portions of the second dielectric film and the second silicon layer to form control gates with exposed side walls which extend in a direction perpendicular to the rows of silicon, etching away portions of the rows of silicon and the first dielectric film to form floating gates which are stacked beneath and self-aligned with control gates;

the source diffusion is formed in the active area of the substrate;

the select and erase gates are formed by forming a third dielectric film on the side walls of the control and floating gates and on the active area of the silicon substrate,

depositing a third silicon layer over the third dielectric film, removing portions of the third silicon layer to form select and erase gates on opposite sides of the stacked gates, with the erase gate being positioned directly above the source diffusion;

the bit line diffusions are formed in the active area of the substrate and are partially overlapped by the select gates;

a bit line which extends in the first direction is formed above the gates; and

bit line contacts are formed to interconnect the bit line and the bit line diffusions.